

Amendments to the Claims:

This Listing of Claims represents the sole remaining claims in the Application. Briefly, previously presented claims 1 – 10 remain herein, following two restriction requirements, and the other claims, 11 – 75, are now cancelled, following withdrawal thereof by the Examiner in the latest Action.

Listing of Claims:

Claims 11 - 75 (cancelled). Please cancel Claims 11 - 75.

1. (previously presented). A method of making a circuitized substrate, said method comprising:

providing a first dielectric layer having a first surface;

forming a first pattern of conductors and a second pattern of conductors spaced from said first pattern and electrically coupled thereto on said first surface of said first dielectric layer;

forming a common conductive line on said first surface of said first dielectric layer electrically connected to each of said conductors of said second pattern of conductors; and

thereafter terminating said electrical connections between each of said conductors of said second pattern of conductors and said common conductive line using a laser.

2. (previously presented). The method of claim 1 further including positioning a second dielectric layer substantially over said first and second patterns of conductors prior to said terminating of said electrical connections.

3. (previously presented). The method of claim 2 wherein said second dielectric layer is provided in substantially liquid form and flowed onto said first dielectric layer.
4. (previously presented). The method of claim 3 wherein said second dielectric layer comprises a soldermask.
5. (previously presented). The method of claim 2 further including using said laser to simultaneously provide openings in said second dielectric layer above respective ones of said electrical connections during said terminating of said connections.
6. (previously presented). The method of claim 5 wherein said laser also partially removes some of said first dielectric layer immediately below said electrical connections during said terminating of said connections.
7. (previously presented). The method of claim 1 wherein said first and second pattern of conductors and said common conductive line are formed using electrolytic plating.
8. (previously presented). The method of claim 1 further including positioning a semiconductor chip on said first dielectric layer and electrically coupling said semiconductor chip to said first pattern of conductors.
9. (previously presented). The method of claim 8 wherein said electrically coupling of said semiconductor chip to said first pattern of conductors is accomplished using a wirebonding operation.
10. (previously presented). The method of claim 8 wherein said semiconductor chip is electrically coupled to said first pattern of conductors using a plurality of solder balls.